

a first terminal coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a second terminal for supplying said first voltage to said first terminal;

a voltage interruption device provided between first and second terminals for

a¹
cont

interrupting an electrical coupling between said first and second terminals; and

a first sacrificial terminal for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

6. (Once Amended) The wafer of claim 5 wherein said fuse is blown when said die draws current in excess of a predetermined value.

9. (Once Amended) A semiconductor die comprising:

a standard Vcc bonding pad coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a secondary Vcc bonding pad;

a³

a fuse interconnected between the standard Vcc bonding pad and the secondary Vcc bonding pad, said secondary Vcc bonding pad supplying said first voltage through said fuse to the standard Vcc bonding pad, said fuse adapted for interrupting electrical coupling

between the secondary Vcc bonding pad and said standard Vcc bonding pads when the die draws current in excess of said fuse breakdown current;

a sacrificial Vcc bonding pad for receiving said first voltage; and

a sacrificial metal bus interconnected between the sacrificial Vcc bonding pad and secondary Vcc bonding pad for receiving said first voltage from the sacrificial Vcc bonding pad and supplying said first voltage to the secondary Vcc bonding pad.

10. (Once Amended) The semiconductor wafer of claim 9 further comprising:

a Vss bonding pad coupled to the circuitry within said die for supplying a second voltage to said circuitry;

a sacrificial Vss bonding pad for supplying the second voltage to the standard Vss bonding pad; and

a sacrificial metal bus which connects the sacrificial Vss bonding pad and the standard Vss bonding pad.

11. (Once Amended) The semiconductor die of claim 10 further comprising:

a passivation layer which is provided with respective openings to the sacrificial Vcc and Vss bonding pads; and

Q3
CONF.
Vcc and Vss sacrificial conductive busses formed over said passivation layer, said Vcc sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vcc sacrificial bonding pad and said Vss sacrificial conductive bus passing through an opening in said passivation layer to connect with said Vss sacrificial bonding pad.

Please add the following new claims:

25. (New) A semiconductor wafer comprising:

at least one first sacrificial conductive line for supplying a first voltage to a plurality of dies fabricated on said wafer;

a plurality of integrated circuit dies fabricated on said wafer, each die comprising:

a4
a first terminal coupled to the circuitry within said die for supplying a first voltage to said circuitry;

a voltage interruption device coupled to said first terminal;

a second terminal coupled to said voltage interruption device, said interruption device for interrupting an electrical coupling between said first and second terminals; and

a first sacrificial terminal electrically coupled to said second terminal for receiving said first voltage from said first sacrificial conductive line and supplying said first voltage to said second terminal.

26. (New) The wafer of claim 25 wherein each die further comprises a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal.

27. (New) The wafer of claim 25 further comprising:

at least one second sacrificial conductive line for supplying a second voltage to said plurality of dies;

each die further comprising:

a third terminal coupled to the circuitry within said die for supplying a second voltage to said circuitry; and

a second sacrificial terminal for receiving said second voltage from said sacrificial second conductive line and supplying said second voltage to said third terminal.

28. (New) The wafer of claim 27 wherein each die further comprises a second on-die sacrificial conductive line provided between the second sacrificial terminal and third terminal.

29. (New) The wafer of claim 25 wherein the voltage interruption device is a fuse.

30. (New) The wafer of claim 29 wherein said fuse is blown when a said die draws current in excess of a predetermined value.

31. (New) The wafer of claim 27 wherein each die further comprises:

a passivation layer having respective openings to the first and second sacrificial terminals, said first and second sacrificial terminals respectively connecting with said first and second sacrificial conductive lines through said openings.

32. The wafer of claim 31 further comprising:

a first on-die sacrificial conductive line provided between the first sacrificial terminal and second terminal; and

a second on-die sacrificial conductive line provided between the third terminal and the second sacrificial terminal.
